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REMARKS

The Official Action and the cited references have again been carefully reviewed. The review indicates that the claims, as amended, recite patentable subject matter and should be allowed. Reconsideration and allowance are therefore respectfully requested.

Prior to addressing the grounds upon which the rejection is based, a summarization of the essentials of the improved invention process for forming dual gate oxides for use in high performance DRAM systems or logic circuits will be provided for purposes of better defining the invention and to draw a clearer line of distinction between the invention process and those processes disclosed in the retained Huang et al. and Kim references.

When producing DRAM devices using a shallow trench isolation (STI) region to obtain a small-size capacitor, wherein gate oxide reliability of support oxides is limited by the thickness of the gate oxide at the AA (active area) corners, wherein careful optimization of the AA oxidation, (sacrificial) oxide, and gate oxidation is necessary to create the required AA corner rounding and the oxide thickness at the AA corner, and wherein in all too many instances the oxide is thinner at the corners than at the AA area, applicants are the first to invent a process for making a high performance DRAM device incorporating different thicknesses of gate oxide by using either angled nitrogen implantation or nitride spacers to create a "shadow effect or area", which limits the nitrogen dose close to the edges of the active area (AA), and wherein the reduction of nitrogen dose leads to an increase gate oxide thickness at the active area adjacent to the shallow trench and increases the threshold of the parasitic corner device and reduces sub Vt (threshold voltage) and junction leakage.

This has unexpectedly been accomplished by:

I) a. forming an active area by depositing over a semiconductor substrate, a patterned hard mask nitride layer

exposing portions of said substrate so as to define an isolation region;

b. etching exposed portions of said substrate using said patterned hard mask nitride layer to form an isolation trench in the isolation region;

c. oxidizing said substrate to form a thermal oxide layer in said isolation trench and capacitor trench;

d. depositing an oxide layer over the thermal oxide layer to fill unfilled portions of said isolation trench;

e. removing said patterned hard mask nitride layer;

f. planarizing said substrate and forming a pad nitride strip;

II) forming a sacrificial gate oxide layer in areas of the semiconductor substrate surface where said pad nitride has been stripped;

III) affecting channel implants in selected areas using resist masks;

IV) affecting a first low dose angled nitrogen implant without using an implant mask to limit the nitrogen dose in the active area to the inner part of the gate area so that the nitrogen dose in the shadow area of the active area is less than the amount of the nitrogen dose implanted in the remaining non-shadowed area to cause

spatial thickness distribution of all exposed oxide areas;

V) affecting masking so that nitrogen ions (N_2^+) to be implanted do not penetrate the masked region; and

VI) affecting a second nitrogen ion implantation by employing a shadow area inducing means at a temperature sufficient to provide a lesser amount of nitrogen ion dosage in the inner part of the gate area so that the angled nitrogen in the shadow area of the active area is less than the amount of nitrogen dose implanted in the remaining non-shadowed area.

Claims 1, 2, and 4-5 were again rejected as being anticipated by Huang et al. or Kim under 35 USC 102(e).

Applicants respectfully traverse these rejections and request reconsiderations for the following reasons.

A careful review of Huang et al. reveals that it disclose using nitrogen implantation techniques for oxynitride formation in semiconductor devices by:

depositing a pad oxide layer on the surface of a silicon substrate;

forming a shallow trench in the substrate;

forming an oxide liner in the shallow trench;

implanting nitrogen into the oxide trench liner and underlying substrate silicon at the oxide/silicon interface; and

filling the trench with oxide.

The key objective of Huang et al. is to suppress both boron penetration into STI oxide and reverse the narrow channel effect (RNCE) in CMOS devices by introducing nitrogen to the STI edges of the p-well. The Huang et al. process also improves isolation performance and is effective to harden the oxide.

Huang et al. makes no reference to or mention of, limiting the dose of nitrogen implantation into edges of the

active area (AA) by use of a "shadow effect or area" created by either angled nitrogen implantation or nitride spacers. Huang et al.'s lack of use of nitrogen implantation so as to create a "shadow effect or area" is apparent from FIGS. 3-5 (despite the fact that Huang et al. may use angled nitrogen implantation per se). This is so because, as can be seen from FIG. 3C of Huang et al., the angled Nitrogen Implant I into trench 306 is directly on the trench and therefore fails to create a shadow area or effect X as shown in FIG. 2 of applicants' invention process due to the height h of the STI oxide 12.

By contrast, as may be seen from FIGS. 2 and 3 of applicants' drawings, the area designated by x shows the use of N_2 implantation so as to limit the nitrogen dose close to the edges of the active area (AA).

Therefore, since at the very minimum, Huang et al. lacks applicants' steps IV and VI, it is abundantly clear that Huang et al. cannot possibly anticipate applicants' claims as amended.

Withdrawal of the rejection is respectfully requested.

Kim too fails to anticipate applicants' claims, as revised for reasons which follow.

Kim disclose a method of manufacturing semiconductor devices having a nitrided silicon substrate using nitrogen ion implantation, comprising:

providing a semiconductor wafer having a silicon substrate and having a layer of sacrificial oxide thereon;

forming a patterned barrier layer on said sacrificial oxide layer;

forming shallow trenches;

implanting nitrogen ions through said sacrificial oxide layer and into said silicon substrate;

removing said sacrificial oxide layer; then

providing a liner oxide layer in said trench;

filling said shallow trenches with a low stress insulating material; and

depositing a layer of high-dielectric constant insulating material on said implanted nitrided silicon substrate.

In Kim, there is no reference to or mention of, the need to limit nitrogen dosage close to edges of the active area of the semiconductor - let alone utilizing angled nitrogen implantation or nitride spacers to create a shadow effect or shadow area to limit the nitrogen dose to lead to an increased gate oxide thickness at the active area adjacent to the shallow trench and increase the threshold of the parasitic corner device and reduce sub Vt and junction leakage.

Thus, Kim too, lacks steps IV and VI of applicants' process, and for at least these reasons, fails to anticipate claims 1,2, 4 and 5 as amended.

Withdrawal of the rejection is respectfully requested.

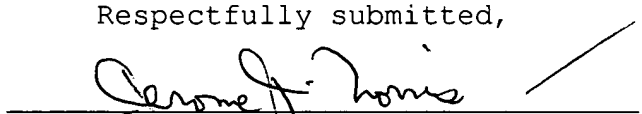
Note is taken of the objection to claim 1 due to inclusion of the phrase "the improvement"; however, inasmuch as the present process is an improvement process, the objection is not well founded in law since improvement patents are clearly authorized by the patent statutes.

Claims 1, 2, 4-5 were rejected under the second paragraph of 35 USC §112 on allegations of indefiniteness, apparently due to lack of understanding of the thrust of applicants' invention - nevertheless, applicants' have made amendments to those sections of the claims in need of more preciseness. Again, applicants are the first to invent a process of making a high performance DRAM device incorporating different thicknesses of gate oxide by using either angled nitrogen implantation or nitride spacers as is shown in FIGS. 2 and 3, to create a "shadow effect or area", which limits the nitrogen dose close to the edges of the active area (AA), and wherein the reduction of nitrogen dose leads to an increased gate oxide thickness at the active area adjacent to the shallow trench isolation region. This innovation increases the threshold of the parasitic corner device and reduces sub Vt (threshold voltage) and junction leakage.

Clearly, neither Huang et al. or Kim alone or in combination anticipate or render obvious applicants' invention since neither of these references utilize either angled nitrogen implantation or nitride spacers shown in applicants' FIGS 2 and 3 to create a "shadow effect or area" which limits the nitrogen dose close to the edges of the active area. If it is felt that interview will foster better grasp of this innovation, it is urged that the Examiner contact the undersigned for a 5 minute interview to clear-up any lack of grasp of the innovation.

In view of the foregoing amendments, remarks and arguments, it is urged that the application is now in condition for allowance and early notification of the same is earnestly solicited.

Respectfully submitted,



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